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PERQ TECHNICHAL NOTE 23
Communication Interfaces

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1. Introduction

This note summarises information given by Brian Rosen about PERQ communication interfaces.

2. Z80 I/O Board

Currently this has only 1K RAM and 8K ROM. The software is to be rewritten (3 months); the board is to be rebuilt and recoded (6-9 months). The new board will have 16K RAM and 4K ROM. About 8K will be used for buffers, of which 2-4K could be stolen for user code. DMA will be provided for PERQ - Z80 transfers, to be handled in 8 byte chunks. (Note that the timescales are for 3R, not ICL).

2.1 GPIB

Our current maximum throughput on the Cambridge Ring via the GPIB is approximately 1.1K bytes/second. The Z80 allocates 32 bytes of its buffer space to the GPIB. When the code is rewritten DMA will be used between the Z80 and GPIB which should increase the throughput to 20K bytes/second. The potential throughput on the new board will be 250K bytes/second.

2.2 HDLC

The recoding of the Z80 will provide access to all the configuration parameters of the SIO which drives the RS 232 interface. This will make it possible to drive the interface synchronously and run HDLC across it. The code will have to be in the PERQ since the Z80 will not have enough memory.

3. PERQ - Unibus/Qbus and Others

The Link hardware used to connect two PERQs can be directly connected to the DEC Unibus DR11 or LSI DRV11. This could be used to run the York X25 software in a front end LSI-11 without modifiction, requiring only the Unix Kernel driver to be rewritten. The link is run by microcode polling.

Interfacing to an alien bus is estimated to take 6 chips and μcode for low throughput, or 24 chips for high throughput.

4. High Speed I/O

Rosen recommends use of a high speed I/O channel for the ring so as not to degrade performance of other devices controlled by the Z80.