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APOLLO DOMAIN v PRIME 750 - SPICE BENCHMARKS

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This note documents the results obtained from running SPICE benchmarks on the Apollo Domain and Prime 750 computers.

1 PREFACE

This note documents the results of running 10 circuits through the circuit analysis program SPICE on both the Apollo Domain and Prime 750 machines.

2 INTRODUCTION

A series of benchmarks have been carried out to compare the computation speed of a number of computer systems sited at the Rutherford Appleton Laboratory (RAL). This note records the results obtained from analysing 10 circuits using the circuit analysis program SPICE on both the Apollo Domain and Prime 750 (RLPB) machines in December 1982.

SPICE is a batch oriented program developed at the University of California primarily to simulate the electrical performance of electronic circuits. The first version was written in FORTRAN and assembler for a CDC 6400 computer. Since then the second version of SPICE has been developed and this has gradually evolved so that SPICE is now available on a number of machines including IBM, DEC VAX and PR1ME.

SPICE consists of approximately 16,000 lines of FORTRAN code (including comments) and internal data storage is of the order of 1M byte, mainly consisting of a two dimensional 200,000 element double precision real array (or 100,000 element double precision complex array).

Apart from its relatively free availability, its success has been built upon the quality of the transistor models. With the increased stringency in design performance of integrated circuits, their operational speed (that is device switching speed) has become a design priority, necessitating the accurate analysis of such circuits at the transistor level. Thus, the demand for circuit analysis programs capable of handling large circuits will increase in the future.

The goal behind this set of benchmarks is to establish the advisability of mounting, on to the Apollo Domain, programs which make heavy demands on a machine's computing resources.

3 COMPUTER DESCRIPTION

3.1 Apollo Domain

The Apollo Domain Computer used in these benchmarks had the following relevant characteristics:

a) 1/2M byte random access store
b) 33M byte Priam Winchester disk
c) software floating point
d) AEGIS 4.1

3.2 Prime 750

The Prime Computer used in these benchmarks had the following relevant characteristics:

a) 3M bytes random access store
b) 2x300M byte CDC 9766 Series disks with separate controllers
c) floating point hardware
d) PRIMOS 18.303

4 BENCHMARKS

Three versions of SPICE were used in the tests. No one version ran on both machines, and although a SPICE 2G version was run on both machines, inspection of the sources showed quite significant differences. The circuits used in the test are described in Table 1 and their full listings are given in the Appendices.

The Apollo tests were run in a single shell window with no other processes running other than those required to normally run the system. Two versions of SPICE were available on the PR1ME and results for both were recorded. PR1ME SPICE benchmarks were run at an ordinary terminal in the same way as any other interactive user of the PR1ME. At RAL, in addition to the central console job, 9 phantom jobs are required to run the system. Each phantom job is equivalent to a logged in user. If the benchmarking job is included, then a minimum number of 10 jobs (not including the central console job) constitutes the most lightly loaded system possible.

The benchmarks were run twice on the PR1ME, once during a lightly loaded period when only the 1 user in addition to the 9 phantoms were running and a second time during the late morning when the system was quite heavily loaded (28 jobs including the 9 phantoms).

The tests were performed singly in the order listed, SPICE 2E tests being performed before SPICE 2G on the PR1ME. Half way through the 2G runs on the PR1ME, the number of user jobs fell from around 30 to 25, the fall occurring at about 11:50am. Between each analysis on the PR1ME, a list of current users was requested. Machine times were used throughout (via the RDYM -ON and RDY -LONG commands) and the tests were performed using control files.

Circuit	Description	No of Transistors	No of Nodes	analysis and output
DIFPAIR	simple differential pair	4	14	ac,dc,tr,pr,pl
RCA3040	RCA 3040 wide band amplifier	11	30	ac,dc,tr,pr,pl
ECLGATE	ECL stacked logic gate	8	36	dc,tr,pr,pl
ASTABLE	simple astable multivibrator	2	11	dc,tr,pr,pl
ADDER	4 bit all NAND gate binary adder	180	442	dc,pr
UA733	UA733 video pre-amplifier	11	23	dc,pr
ECLINV	emitter coupled logic inverter	4	17	dc,tr,pr,pl
SCHMITT	ECL compatible schmitt trigger	4	17	dc,tr,pr,pl
UA741	UA 741 operational amplifier	22	49	dc,ac,tr,pr,pl
SENTST7	sensitivity test 7	1	11	dc,se,pr

Table 1: Circuits used in the SPICE Benchmarks

ac - ac analysis performed;
dc - dc analysis performed;
pr - printed output filed on to disk;
tr - transient analysis performed;
se - small signal sensitivity;
pl - plotted (lineprinter) output filed on to disk;

5 RESULTS

5.1 Lightly Loaded Prime versus Domain

Contained in Table 2 are the results of running the SPICE benchmarks on a PRIME with a minimum number of user jobs (10) compared with the results obtained from analysing the same circuits on the Apollo Domain.

CIRCUIT	APOLLO DOMAIN SPICE 2G.1D		PRIME 750 SPICE 2E.3		PRIME 750 SPICE 2G.5	
	cpu time (secs)	real time (secs)	cpu time (secs)	real time (secs)	cpu time (secs)	real time (secs)
DIFPAIR	171	203	21	25	20	26
RCA3040	426	461	37	43	39	47
ECLGATE	458	498	37	44	41	48
ASTABLE	246	281	19	25	25	31
ADDER	1034	1081	131	145	177	195
UA733	26	62	5	10	5	10
ECLINV	130	167	15	20	14	19
SCHMITT	170	205	15	20	16	22
UA741	894	939	61	69	78	88
SENTST7	18	52	4	7	3	8

Table 2: Domain versus Prime 750 with minimum jobs
(1 user, 9 phantoms and central console)

5.2 Quite Heavily Loaded Prime versus Domain

Table 3 contains the results of running the SPICE benchmarks on a quite heavily loaded PRIME compared with the results obtained from analysing the same circuits on the Apollo Domain.

CIRCUIT	APOLLO DOMAIN SPICE 2G.1D		PRIME 750 SPICE 2E.3			PRIME 750 SPICE 2G.5		
	cpu time (secs)	real time (secs)	cpu time (secs)	real time (secs)	no. of users	cpu time (secs)	real time (secs)	no. of users
DIFPAIR	171	203	23	77	29	23	159	32
RCA3040	426	461	39	204	29	43	302	32
ECLGATE	458	498	39	142	31	44	267	30
ASTABLE	246	281	21	126	29	27	164	31
ADDER	1034	1081	141	611	29	185	576	30
UA733	26	62	6	59	29	6	30	25
ECLINV	130	167	17	68	29	14	30	24
SCHMITT	170	205	16	99	30	17	33	23
UA741	894	939	66	262	30	80	164	24
SENTST7	18	52	5	87	31	4	26	24

Table 3: Domain versus Prime 750 (quite heavily loaded)
(30 users = 1 user + 9 phantoms + 20 other users)

6 ANALYSIS

6.1 Lightly Loaded Prime v Domain - Relative Performance

Table 4 show how much longer (relatively) the Apollo Domain version of SPICE 2G takes to analyse the same circuit compared with the PR1ME 750 SPICE 2G when the PR1ME has a minimum number of user jobs. In summary a circuit which takes 10 minutes on a PR1ME with only one user (plus 9 phantoms) would take 84 minutes on an Apollo Domain. The variation in relative times range from 10.4 to 5.5, the lower values occurring where only dc analyses were performed. The number of variables (analysis performed, number of nodes, size of resulting output file, disk I/O times etc.) is too large to be able to isolate the reason for the 'lower' results.

CIRCUIT	PRIME 750 SPICE 2G.5			APOLLO DOMAIN SPICE 2G.1D	
	no. of users	relative cpu time	relative real time	relative cpu time	relative real time
DIFPAIR	10	1	1	8.6	7.8
RCA3040	10	1	1	10.9	9.8
ECLGATE	10	1	1	11.2	10.4
ASTABLE	10	1	1	9.8	9.1
ADDER	10	1	1	5.8	5.5
UA733	10	1	1	5.2	6.2
ECLINV	10	1	1	9.3	8.8
SCHMITT	10	1	1	10.6	9.3
UA741	10	1	1	11.5	10.7
SENTST7	10	1	1	6.0	6.5
Average	10	1	1	8.9	8.4

Table 4: Relative speeds with minimum jobs

6.2 Quite Heavily Loaded Prime v Domain - Relative Performance

Table 5 shows how much longer the Apollo Domain version of SPICE 2G takes to analyse the same circuit compared with the PR1ME 750 SPICE 2G when the PR1ME is quite heavily loaded. In summary, a circuit which takes 10 minutes on the PR1ME would take 30 minutes on an Apollo Domain. The variation ranges from 1.7 to 6.2, the 'longer' results occurring with ECLINV, SCHMITT and UA741. No reason for this has been isolated.

CIRCUIT	PRIME 750 SPICE 2G.5			APOLLO DOMAIN SPICE 2G.1D	
	no. of users	relative cpu time	relative real time	relative cpu time	relative real time
DIFPAIR	32	1	1	7.4	1.3
RCA3040	32	1	1	9.9	1.5
ECLGATE	30	1	1	10.4	1.9
ASTABLE	31	1	1	9.1	1.7
ADDER	30	1	1	5.6	1.9
UA733	25	1	1	4.3	2.1
ECLINV	24	1	1	9.3	5.6
SCHMITT	23	1	1	10.0	6.2
UA741	24	1	1	11.2	5.7
SENTST7	24	1	1	4.5	2.0
Average	28	1	1	8.2	3.0

Table 5: Relative speeds with many jobs

6.3 Output File Size and Disk I/O

Table 6 was produced in an attempt to isolate the 6 'odd' results obtained. This table shows the size of the output files and PR1ME disk I/O times (disk I/O time is not available on the Apollo Domain). The following conclusions may be drawn:

a. Disk I/O on the PR1ME bears no simple relation to disk size of the resulting output file.

b. Disk I/O is virtually the same for a minimally loaded PR1ME irrespective of disk size of the output file.

But these conclusions fail to provide a theory as to the cause(s) of the 'odd' results.

CIRCUIT	FILE SIZES			PRIME DISK I/O			
				LIGHT LOADING		HEAVY LOADING	
	APOLLO DOMAIN 2G.1D	PRIME 750 2G.5	PRIME 750 2E.3	2G.5 (secs)	2E.3 (secs)	2G.5 (secs)	2E.3 (secs)
DIFPAIR	66,144	64,262	64,491	3.30	3.45	14.72	8.51
RCA3040	69,674	67,700	67,790	3.75	3.17	25.60	8.17
ECLGATE	48,437	46,780	47,300	3.44	3.99	22.10	10.04
ASTABLE	28,683	27,827	28,247	3.55	3.65	13.01	9.47
ADDER	98,569	94,600	85,985	3.91	4.15	25.68	21.84
UA733	11,095	10,293	9,631	3.39	3.66	11.61	12.42
ECLINV	31,466	30,258	30,964	3.39	3.70	4.77	7.39
SCHMITT	30,054	29,132	29,581	3.65	3.90	5.07	15.48
UA741	75,386	73,159	72,858	3.45	3.62	5.94	16.30
SENTST7	8,492	7,867	7,642	3.27	3.64	12.00	16.99

Table 6: Output File Size and Disk I/O Times

7 CONCLUSIONS

The following points should be borne in mind:

1. The Apollo Domain used in this set of tests did not have floating point hardware. This is an available option and Apollo claim that it should give an overall improvement of 60%. The Domain would then be able to provide a response roughly equivalent to that experienced by a user timesharing with 30 others on a PRIME 750.

2. The Apollo Domain hardware is costed at $31,119 (incl. vat) With the floating point hardware it would cost $34,638 (incl. vat) This per node price falls as more diskless nodes are connected together.

3. No identical version of SPICE was run on both machines.

Even when the PRIME system is quite heavily loaded, it provides results in a third of the time that it takes the Apollo Domain. Furthermore, a user can adjust his working time so as to utilise the machine when there are fewer users, thus reducing the ratio to about an eighth of the time it takes the Apollo Domain.

It is true that the Domain does have a fairly predictable response time, but this is not necessarily attractive when the overall response time is so slow. Furthermore, in situations where the time shared system is noticeably slower than normal, he can always hope that his next run must be faster than the last one. In this case the unpredictable nature may be more attractive.

It may be concluded that heavy computational programs are not suitable for the Apollo Domain. However, a single user machine costing a quarter of the price of an Apollo Domain with floating point hardware might be closer to being a cost effective alternative to a timeshared minicomputer when other attributes (such as concurrent processes in separate visual windows) are taken into account.

8 APPENDIX A DIFPAIR - Simple Differential Pair

```
DIFPAIR CKT - SIMPLE DIFFERENTIAL PAIR
.WIDTH IN=72
.OPT ACCT LIST NODE LVLCOD=1
.TF V(5) VIN
.DC VIN -0.25 0.25 0.005
.AC DEC 10 1 10GHZ
.TRAN 5NS 500NS
VIN 1 0 SIN(0 0.1 5MEG) AC 1
VCC 8 0 12
VEE 9 0 -12
Q1 4 2 6 QNL
Q2 5 3 6 QNL
RS1 1 2 1K
RS2 3 0 1K
RC1 4 8 10K
RC2 5 8 10K
Q3 6 7 9 QNL
Q4 7 7 9 QNL
RBIAS 7 8 20K
.MODEL QNL NPN(BF=80 RB=100 CCS=2PF TF=0.3NS TR=6NS CJE=3PF CJC=2PF
+   VA=50)
.PRINT DC V(4) V(5)
.PLOT DC V(5)
.PRINT AC VM(5) VP(5)
.PLOT AC VM(5) VP(5)
.PRINT TRAN V(4) V(5)
.PLOT TRAN V(5)
.END
```

9 APPENDIX B RCA3040 - RCA 3040 Wide Band Amplifier

```
RCA3040 CKT - RCA 3040 WIDEBAND AMPLIFIER
.WIDTH IN=72
.OPT ACCT LIST NODE LVLCOD=1
.DC VIN -0.25 0.25 0.005
.AC DEC 10 1 10GHZ
.TRAN 0.5NS 50NS
VIN 1 0 SIN(0 0.1 50MEG) AC 1
VCC 2 0 15.0
VEE 3 0 -15.0
RS1 30 1 1K
RS2 31 0 1K
R1 6 3 4.8K
R2 5 3 4.8K
R3 9 3 0.811K
R4 8 3 2.17K
R5 8 0 0.82K
R6 2 14 1.32K
R7 2 12 4.5K
R8 2 15 1.32K
R9 16 0 5.25K
R10 17 0 5.25K
Q1 2 31 6 QNL
Q2 2 30 5 QNL
Q3 10 5 7 QNL
Q4 11 6 7 QNL
Q5 14 12 10 QNL
Q6 15 12 11 QNL
Q7 12 12 13 QNL
Q8 13 13 0 QNL
Q9 7 8 9 QNL
Q10 2 15 16 QNL
Q11 2 14 17 QNL
.MODEL QNL NPN(BF=80 RB=100 CCS=2PF TF=0.3NS TR=6NS CJE=3PF CJC=2PF
+   VA=50)
.PRINT DC V(16) V(17)
.PLOT DC V(17)
.PRINT AC VM(17) VP(17)
.PLOT AC VM(17) VP(17)
.PRINT TRAN V(16) V(17)
.PLOT TRAN V(17)
.END
```

10 APPENDIX C ECLGATE - ECL Stacked Logic Gate

```
ECLGATE CKT - ECL STACKED LOGIC GATE
.WIDTH IN=72
.OPT ACCT LIST NODE LVLCOD=1
.DC VIN -2 0 0.02
.TRAN 0.2NS 20NS
VEE 15 0 -6
VIN 16 0 PULSE(-1.8 -0.8 1NS 1NS 1NS)
VGATE 17 0 PULSE(-0.8 -1.8 5NS 1NS 1NS 5NS)
RS1 16 1 50
Q1 2 1 3 QND
Q2 0 9 3 QND
RC 0 2 100
RS2 17 4 50
Q3 0 4 5 QND
R1 5 6 60
R2 6 15 820
Q4 3 6 7 QND
RE 7 15 280
Q5 0 12 7 QND
R5 0 8 100
Q6 0 8 9 QND
R3 9 15 2K
D1 8 10 D1
R6 10 11 60
Q7 0 11 12 QND
R4 12 15 2K
D2 11 13 D1
R7 13 15 720
Q8 0 2 14 QND
RL 14 15 560
.MODEL D1 D(RS=40 TT=0.1NS CJO=0.9PF)
.MODEL QND NPN(BF=50 RB=70 RC=40 CCS=2PF TF=0.1NS TR=10NS CJE=0.9PF
+   CJC=1.5PF PC=0.85 VA=50)
.PRINT DC V(6) V(14)
.PLOT DC V(14)
.PRINT TRAN V(6) V(14)
.PLOT TRAN V(14) V(16) V(17) V(6)
.END
```

11 APPENDIX D ASTABLE - A Simple Astable Multivibrator

```
ASTABLE CKT - A SIMPLE ASTABLE MULTIVIBRATOR
.WIDTH IN=72
.OPT ACCT LIST NODE LVLCOD=1
.TRAN 0.1US 10US
VIN 5 0 PULSE(0 5 0 1US 1US 100US 100US)
VCC 6 0 5
RC1 6 1 1K
RC2 6 2 1K
RB1 6 3 30K
RB2 5 4 30K
C1 1 4 150PF
C2 2 3 150PF
Q1 1 3 0 QSTD
Q2 2 4 0 QSTD
.MODEL QSTD NPN(IS=1.0E-16 BR=50 BR=0.1 RB=50 RC=10 TF=0.12NS TR=5NS
+   CJE=0.4PF PC=0.8 ME=0.4 CJE=0.5PF PC=0.8 MC=0.333 CCS=1PF VA=50)
.PRINT TRAN V(1) V(2) V(3) V(4)
.PLOT TRAN V(2) V(3) V(4) V(1)
.END
```

12 APPENDIX E ADDER - Fourbit All NAND Gate Binary Adder

```
ADDER - 4 BIT ALL-NAND-GATE BINARY ADDER
.WIDTH IN=72
.SUBCKT NAND 1 2 3 4
*    NODES
Q1 9 5 1 QMOD
D1CLAMP 0 1 DMOD
Q2 9 5 2 QMOD
D2CLAMP 0 2 DMOD
RB 4 5 4K
R1 4 6 1.6K
Q3 6 9 8 QMOD
R2 8 0 1K
RC 4 7 130
Q4 7 6 10 QMOD
DVBEDROP 10 3 DMOD
Q5 3 8 0 QMOD
.ENDS NAND
.SUBCKT ONEBIT 1 2 3 4 5 6
*    NODES
X1 1 2 7 6 NAND
X2 1 7 8 6 NAND
X3 2 7 9 6 NAND
X4 8 9 10 6 NAND
X5 3 10 11 6 NAND
X6 3 11 12 6 NAND
X7 10 11 13 6 NAND
X8 12 13 4 6 NAND
X9 11 7 5 6 NAND
.ENDS ONEBIT
.SUBCKT TWOBIT 1 2 3 4 5 6 7 8 9
*    NODES
*            CARRY-IN, CARRY-OUT, VCC
X1 1 2 7 5 10 9 ONEBIT
X2 3 4 10 6 8 9 ONEBIT
.ENDS TWOBIT
.SUBCKT FOURBIT 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
*    NODES
*            OUTPUT - BIT0 / BIT1 / BIT2 / BIT3, CARRY-IN, CARRY-OUT, V
CC
X1 1 2 3 4 9 10 13 16 15 TWOBIT
X2 5 6 7 8 11 12 16 14 15 TWOBIT
.ENDS FOURBIT
***
***  DEFINE NOMINAL CIRCUIT
***
.MODEL DMOD D
.MODEL QMOD NPN(BF=75 RB=100 CJE=1PF CJC=3PF)
VCC 99 0 DC 5V
VIN1A 1 0 PULSE(0 3 0 10NS 10NS   10NS   50NS)
VIN1B 2 0 PULSE(0 3 0 10NS 10NS   20NS  100NS)
VIN2A 3 0 PULSE(0 3 0 10NS 10NS   40NS  200NS)
VIN2B 4 0 PULSE(0 3 0 10NS 10NS   80NS  400NS)
```

```
VIN3A 5 0 PULSE(0 3 0 10NS 10NS  160NS  800NS)
VIN3B 6 0 PULSE(0 3 0 10NS 10NS  320NS 1600NS)
VIN4A 7 0 PULSE(0 3 0 10NS 10NS  640NS 3200NS)
VIN4B 8 0 PULSE(0 3 0 10NS 10NS 1280NS 6400NS)
X1 1 2 3 4 5 6 7 8 9 10 11 12 0 13 99 FOURBIT
RBIT0 9 0 1K
RBIT1 10 0 1K
RBIT2 11 0 1K
RBIT3 12 0 1K
RCOUT 13 0 1K
.OP
.OPT ACCT LIST NODE LVLCOD=1
.END
```

13 APPENDIX F UA733 - UA733 Video Amplifier

```
UA733 CKT - UA 733 VIDEO PREAMPLIFIER
.WIDTH IN=72
.OPT ACCT LIST NODE LVLCOD=1
VCC 11 0 8
VEE 9 0 -8
Q1 3 1 4 Q1
Q2 14 2 13 Q1
Q3 17 14 16 Q1
Q4 18 3 16 Q1
Q5 11 18 19 Q1
Q6 11 17 22 Q1
Q7 6 7 8 Q1
Q8 7 7 10 Q1
Q9 16 7 15 Q1
Q10 19 7 20 Q1
Q11 22 7 21 Q1
R1 1 0 51
R2 2 0 51
R3 11 3 2.5K
R4 11 14 2.4K
R5 4 5 50
R6 13 12 50
R7 5 6 590
R8 12 6 590
R9 11 7 10K
R10 11 17 1.1K
R11 11 18 1.1K
R12 3 19 7K
R13 14 22 7K
R14 8 9 300
R15 10 9 1.4K
R16 15 9 300
R17 20 9 400
R18 21 9 400
.MODEL Q1 NPN(BF=100 BR=2 IS=0.9901E-15)
.END
```

14 APPENDIX G ECLINV - Emitter Coupled Logic Inverter

```
ECLINV CKT - EMITTER COUPLED LOGIC INVERTER
.WIDTH IN=72
.OPT ACCT LIST NODE LVLCOD=1
.TRAN 0.2NS 20NS
VIN 1 0 PULSE(-1 -1.8 1NS 1NS 1NS 8NS 20NS)
VEE 8 0 -5
VREF 6 0 -1.4
Q1 3 2 4 QSTD
Q2 5 6 4 QSTD
Q3 0 5 7 QSTD
Q4 0 5 7 QSTD
RIN 1 2 50
RC1 0 3 80
RC2 0 5 135
RE 4 8 340
RTH1 7 8 125
RTH2 7 0 85
CLOAD 7 0 5PF
.MODEL QSTD NPN(IS=1.0E-16 BR=50 BR=0.1 RB=50 RC=10 TF=0.12NS TR=5NS
+   CJE=0.4PF PC=0.8 ME=0.4 CJE=0.5PF PC=0.8 MC=0.333 CCS=1PF VA=50)
.PRINT TRAN V(1) V(3) V(5) V(7) I(VIN)
.PLOT TRAN V(3) V(5) V(7) V(1) I(VIN)
.END
```

15 APPENDIX H SCHMITT - ECL Compatible Schmitt Trigger

```
SCHMITT CKT - ECL COMPATIBLE SCHMITT TRIGGER
.WIDTH IN=72
.OPT ACCT LIST NODE LVLCOD=1
.TRAN 10NS 1000NS
VIN 1 0 PULSE(-1.6 -1.2 10NS 400NS 400NS 100NS 10000NS)
VEE 8 0 -5
RIN 1 2 50
RC1 0 3 50
R1 3 5 185
R2 5 8 760
RC2 0 6 100
RE 4 8 260
RTH1 7 8 125
RTH2 7 0 85
CLOAD 7 0 5PF
Q1 3 2 4 QSTD OFF
Q2 6 5 4 QSTD
Q3 0 6 7 QSTD
Q4 0 6 7 QSTD
.MODEL QSTD NPN(IS=1.0E-16 BF=50 BR=0.1 RB=50 RC=10 TF=0.12NS TR=5NS
+   CJE=0.4PF PE=0.8 ME=0.4 CJC=0.5PF PC=0.8 MC=0.333 CCS=1PF VA=50)
.PRINT TRAN V(1) V(3) V(5) V(6)
.PLOT TRAN V(3) V(5) V(6) V(1)
.END
```

16 APPENDIX I UA741 - UA741 Operational Amplifier

```
UA741 CKT - UA 741 OPERATIONAL AMPLIFIER
.WIDTH IN=72
.OPT ACCT LIST NODE LVLCOD=1
.DC VIN -0.25 0.25 0.005
.AC DEC 10 1 10GHZ
.TRAN 2.5US 250US
VCC 27 0 15
VEE 26 0 -15
VIN 30 0 SIN(0 0.1 10KHZ) AC 1
RS1 2 30 1K
RS2 1 0 1K
RF 24 2 100K
R1 10 26 1K
R2 9 26 50K
R3 11 26 1K
R4 12 26 3K
R5 15 17 39K
R6 21 20 40K
R7 14 26 50K
R8 18 26 50
R9 24 25 25
R10 23 24 50
R11 13 26 50K
COMP 22 8 30PF
Q1 3 1 4 QNL
Q2 3 2 5 QNL
Q3 7 6 4 QPL
Q4 8 6 5 QPL
Q5 7 9 10 QNL
Q6 8 9 11 QNL
Q7 27 7 9 QNL
Q8 6 15 12 QNL
Q9 15 15 26 QNL
Q10 3 3 27 QPL
Q11 6 3 27 QPL
Q12 17 17 27 QPL
Q14 22 17 27 QPL
Q15 22 22 21 QNL
Q16 22 21 20 QNL
Q17 13 13 26 QNL
Q18 27 8 14 QNL
Q19 20 14 18 QNL
Q20 22 23 24 QNL
Q21 13 25 24 QPL
Q22 27 22 23 QNL
Q23 26 20 25 QPL
.MODEL QNL NPN(BF=80 RB=100 CCS=2PF TF=0.3NS TR=6NS CJE=3PF CJC=2PF
+   VA=50)
.MODEL QPL PNP(BF=10 RB=20 TF=1NS TR=20NS CJE=6PF CJC=4PF VA=50)
.PRINT DC V(8) V(24)
.PLOT DC V(24)
.PRINT AC VM(24) VP(24)
```

```
.PLOT AC VM(24) VP(24)
.PRINT TRAN V(8) V(24)
.PLOT TRAN V(24) V(8)
.END
```

17 APPENDIX J SENTST7 - Sensitivity Test 7

```
SENTST7 - SENSITIVITY TEST 7
.WIDTH IN=72
.OPT ACCT LIST NODE LVLCOD=1
.SENS V(5,6)
VCC 7 0 DC -10
VIN 1 0 DC -518MV
R1 1 2 10
R2 5 4 10
R3 3 0 10
Q1 3 2 4 Q1
R4 7 6 100
R5 6 5 1
.MODEL Q1 PNP(BF=100 BR=100 RB=10 RC=10 RE=10 IS=1.0E-14 VA=50)
.END
```