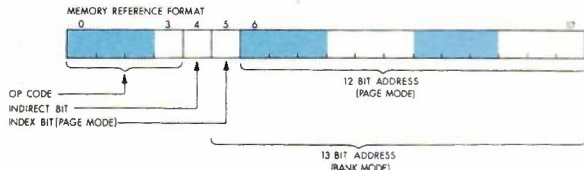


MEMORY REFERENCE INSTRUCTIONS*



Mnemonic	Code	Operation	Memory Cycles	Execute Time (Microsec.)
CAL	00	JMS Absolute 20s	2	1.6
DAC	04	Deposit AC	2	1.6
JMS	10	Jump to Subroutine	2	1.6
DZM	14	Deposit Zero in Memory	2	1.6
LAC	20	Load AC	2	1.6
XOR	24	Exclusive OR	2	1.6
ADD	30	Add (1's Complement)	2	1.85
TAD	34	Add (2's Complement)	2	1.6
XCT	40	Execute	1+	.8+
ISZ	44	Increment and skip if zero	3	2.4
AND	50	AND	2	1.6
SAD	54	Skip if AC ≠ Memory	2	1.6
JMP	60	Unconditional jump	1	.8

*Add 1 cycle for indirect addressing or auto indexing (no extra time required for indexing).

Indirect Addressing through locations 10s-17s will cause these locations to increment on each access.

Special Op Codes

EAE	64	Extended Arithmetic	1-2	1.325-7.685
IOT	70	Input/Output Transfer	1	2.21-5.02
FPP	71	Floating Point Processor	1-4	5.0-18.3
IND	72	Index Group	1	1.6
OPR	74	Operate Group	1	.8

OPERATE INSTRUCTIONS

NOP	740000	Operate group, no operation	1	.8
CMA	740001	Ones Complement AC	1	.8
CML	740002	Complement L	1	.8
OAS	740004	OR AC switches to AC	1	.8
RAL	740010	Rotate AC and L one left	1	.8
RAR	740020	Rotate AC and L one right	1	.8
IAC	740030	Increment the AC	1	.8
HLT	740040	Halt	1	.8
SMA	740100	Skip if AC < 0	1	.8
SZA	740200	Skip if AC = 0	1	.8
SNL	740400	Skip if L ≠ 0	1	.8
SKP	741000	Unconditional Skip	1	.8
SPA	741100	Skip if AC ≥ 0	1	.8
SNA	741200	Skip if AC ≠ 0	1	.8
SZL	741400	Skip if L = 0	1	.8
RTL	742010	Rotate AC and L two places left	1	.8
RTR	742020	Rotate AC and L two places right	1	.8
SWHA	742030	Swap halves of the AC	1	.8
CLL	744000	Clear L	1	.8
CLA	750000	Clear AC	1	.8
LAW	76XXXX+n	Load the AC with 760000+n (0 ≤ n ≤ 17777)	1	.8

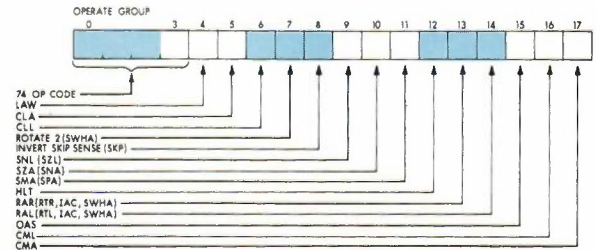
Operate Combinations Found In Permanent Symbol Table of MACRO 15

TCA	740031	Two's complement accumulator	1	.8
STL	744002	Set L	1	.8
RCL	744010	Clear L, rotate AC and L one left	1	.8
RCR	744020	Clear L, rotate AC and L one right	1	.8
CLC	750001	Clear and complement AC	1	.8
LAS	750004	Load AC from Console switches	1	.8
GLK	750010	L → AC 17	1	.8

OPERATE INSTRUCTIONS COMBINING CHART

1			2		3			4
SNL	SZA	SMA	CLL	CLA	BAS	CMA	IAC	HLT
SZL	SNA	SPA			RAR			
SKP					RAL			
					RTR			
					RTL			
					SWHA			

- Instructions occur in order 1 through 4.
- Instructions may be combined unless they are in different boxes in the same column.
- The following skips are combined as if ORed: SNL, SZA, SMA.
- The following skips are combined as if ANDeD: SZL, SNA, SPA.
- CML occurs at time 3 and can be combined normally with everything except IAC and Rotates.
- CML combined with IAC executes as a CMLISTL and therefore should not be used.
- CML combined with a rotate will cause the new state of the L to be an OR of the compliment of the L and the state rotated in and therefore should not be used.
- SWHA combined with CLA will leave the AC in the same state as it held before the instruction was executed and so should not be used.
- SWHA and Rotates will cause the following to be ignored: OAS, CMA, IAC.
- LAW will cause all other microcodes to be ignored.
- All illegal combinations not otherwise mentioned will correspond to some correct microcode of different meaning and be executed as such.



Condition	Code
AC > 0	SPA SNA
AC = 0	SPA
AC = 0	SZA
AC < 0	SMA SZA
AC < 0	SMA
AC = 0	SNA

INDEX INSTRUCTIONS

REGISTER CONTROL INSTRUCTIONS

Mnemonic	Code	Operation	Memory Cycles	Execute Time (Microsec.)
AXS+n	725XXX±n	Add ±n (0 ≤ n ≤ 377) to index register and skip if ≥ limit register	1*	1.6
AXR+n	737XXX±n	Add n to the index register	1*	1.6
AAC+n	723XXX±n	Add n to the accumulator	1*	1.6

REGISTER TRANSFER INSTRUCTIONS

PAX	721000	Place accumulator in index register	1*	1.6
PAL	722000	Place accumulator in limit register	1*	1.6
PXA	724000	Place index register in accumulator	1*	1.6
PXL	726000	Place index register in limit register	1*	1.6
PLA	730000	Place limit register in accumulator	1*	1.6
PLX	731000	Place limit register in index register	1*	1.6
CLX	735000	Clear the index register	1*	1.6
CLLR	736000	Clear the limit register	1*	1.6

*For these eleven instructions, although only one memory cycle is required, the CPU requires another cycle to complete the operation. Each CPU cycle is completed within 800 nanoseconds.

EAE INSTRUCTIONS

EAE	640000	EAE group, no operation	1.325
MUL	653122	Multiply, unsigned	2.915+-.265L***
MULS	657122	Multiply, signed	
DIV	640323	Divide, unsigned	
DIVS	644323	Divide, signed	
IDIV	653323	Integer divide, unsigned	2.915+-.265m**
IDIVS	657323	Integer divide, signed	
FRDIV	650323	Fractional divide, unsigned	2.915+-.1325h*
FRDIVS	654323	Fractional divide, signed	
NORM	640444	Normalize, unsigned	1.325 set up instructions
NORMS	660444	Normalize, signed	
LRS	6405xx+n	Long right shift	1.325 set up instructions
LRSS	6605xx+n	Long right shift, signed	
LLS	6406xx+n	Long left shift	1.325 set up instructions
LLSS	6606xx+n	Long left shift, signed	
ALS	6407xx+n	Accumulator left shift	1.325 set up instructions
ALSS	6607xx+n	Accumulator left shift, signed	
OSC	640001	OR SC to AC12-17	1.325 set up instructions
OMQ	640002	OR MQ to AC	
CMQ	640004	Complement MQ	1.325 set up instructions
†CLAC	641000	Clear AC	
†OAC	642000	OR AC to MQ	1.325 set up instructions
ABS	644000	Load AC with absolute value of AC	
CLQ	650000	Clear MQ	1.325 set up instructions
†SLK	660000	Move sign (AC00) to link	

Combined EAE Set Up Instructions Recognized by MACRO 15

LACS	641001	Load AC12-17 with SC	1.325
LACQ	641002	Load AC 0-17 with MQ	
LMQ	652000	Load MQ with AC	1.325
GSM	664000	Sign → Link, AC → AC	

*Where "h" is the number of steps the instruction must carry out $0 \leq h \leq 36_{10}$

**Where "m" is the number of steps a divide instruction carries out $0 \leq m \leq 19_{10}$

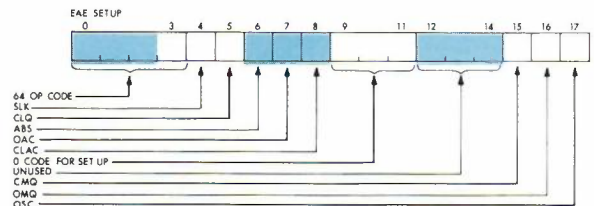
***Where "L" is the number of steps a multiply instruction carries out $0 \leq L \leq 18_{10}$

†Not recognized by the permanent symbol table of MACRO 15

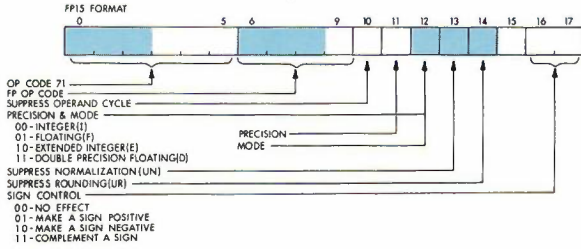
EAE Set Up Combining Chart

1	2	3	4
ABS SLK CLQ	OAC	CMQ CLAC	OMQ OSC

- Order of events is from 1 to 4.
- Any EAE Set Up can be combined with any other EAE Set Up.
- EAE Set Up and other EAE instructions should not be combined.



FP15 INSTRUCTIONS



General Case FP OP Codes

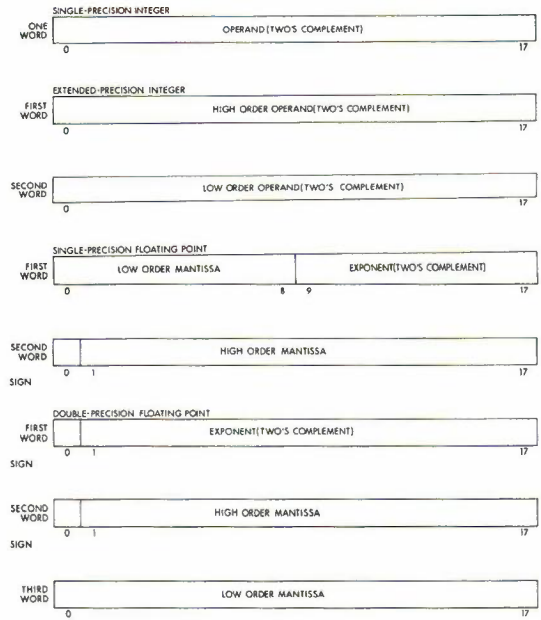
SB	710400	Subtract, FMA→Arg→FMA	6.2-11.2
RS	711000	Reverse Subtract, Arg→FMA→FMA	6.2-11.2
MP	711400	Multiply, Arg×FMA→FMQ, FMA	14.1-18.6
DV ¹	712000	Divide, FMA/Arg→FMA, r→FMQ	11.8-18.3
RD ¹	712400	Reverse Divide, Arg/FMA→FMA, r→FMQ	11.8-18.3
LD ²	713000	Load, Arg→FMA	6.6-9.5
ST ³	713600	Store, FMA→Arg	6.6-9.1
LF ⁴	714010	Load and Float, Arg→FMA	6.6-11.2
LX ⁵	714460	Load floating and Fix, Arg→FMA	11.0-12.4
LQ ²	715000	Load and Swap, Arg→FMQ, FMQ→FMA	6.6-14.0
AD	716000	Add, Arg+FMA→FMA	6.6-9.3

1. Normalization must not be suppressed for DV or RD.
2. Rounding is irrelevant for LD and LQ and therefore should be suppressed for floating numbers.
3. Rounded Double Stores (DST) are illegal. URDST must be used.
4. LF arguments must be integer, rounding is irrelevant and therefore should be suppressed.
5. LX arguments must be floating, normalization is irrelevant and therefore should be suppressed.

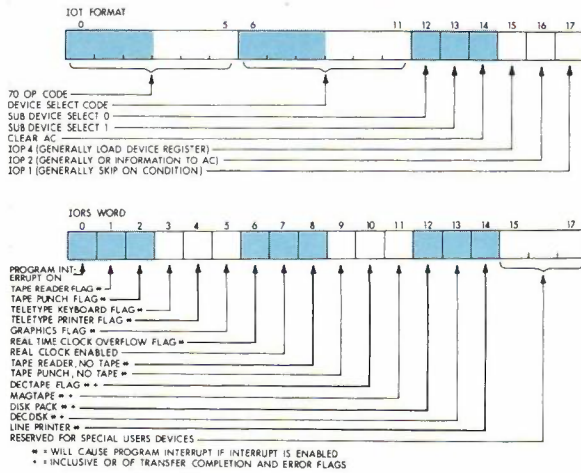
Particular Case FP Instructions

FPT	710314	Floating Point Test	5.0
FZR	711200	Zero EPA (A SIGN) FMA	5.2
FAB	713271	Make A SIGN positive (Absolute Value)	5.2
FNG	713272	Make A SIGN Negative	5.2
FCM	713273	Complement A SIGN	5.2
FNM	713250	Normalize EPA (A SIGN) FMA	8.4
FLA	714210	Float FMA	8.2
UNFLA	714230	Unnormalized, Float FMA	5.3
FXA	714660	Fix EPA, FMA	8.3
URFXA	714670	Unrounded, Fix EPA, FMA	8.3
SWQ	715250	Swap FMA and FMQ	5.5
UNSWQ	715270	Unnormalized Swap FMA and FMQ	5.3
LJE	715400	Load JEA Register	6.6
SJE	715600	Store JEA Register	6.6
BZA	716601	Branch on Zero FMA	5.2
BMA	716602	Branch on Minus FMA	5.2
BLE	716603	Branch if FMA≤0	5.2
BPA	716604	Branch on Positive FMA	5.2
BRU	716606	Branch Unconditional	5.2
BNA	716610	Branch on Non-Zero FMA	5.2
BAC	716620	Branch if Carry Out of FMA	5.2

Data Formats



INPUT/OUTPUT TRANSFER INSTRUCTIONS



Mnemonic ¹	Code	Operation	Execute Time (Microseconds) ²
—	700304	OR status to AC	3.96-5.02
IORS	700314	Read status	3.96-5.02
CAF	703302	Clear flags	3.21-4.27
EBA	707764	Enable bank addressing	3.96-5.02
DBA	707762	Disable bank addressing	3.21-4.27
SBA	707761	Skip if bank addressing	2.21-3.27
SK15	707741	Skip if PDP-15	2.21-3.27

PROGRAM INTERRUPT

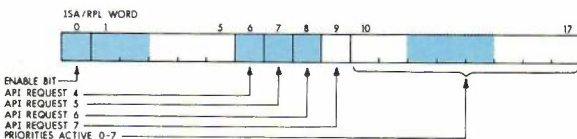
IOP	700002	Turn interrupt off	3.21-4.27
ION	700042	Turn interrupt on	3.21-4.27

TYPE KW15 REAL-TIME CLOCK

CLSF	700001	Skip on clock flag	2.21-3.27
CLOF	700004	Disable clock	3.96-5.02
CLON	700044	Enable clock	3.96-5.02

TYPE KA15 AUTOMATIC PRIORITY INTERRUPT

RES	707742	Restore	3.21-4.27
DBK	703304	Debreak	3.96-5.02
DBR	703344	Debreak and restore	3.96-5.02
SPI	705501	Skip on priorities inactive	2.21-3.27
ISA	705504	Initiate selected activity	3.96-5.02
—	705502	OR priority levels into AC	3.21-4.27
RPL	705512	Load priority levels into AC	3.21-4.27
EBI	705521	Enable breaks	2.21-3.27
DBI	705522	Disable breaks	3.21-4.29



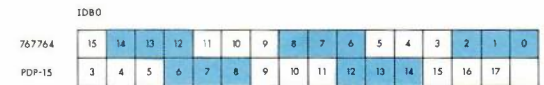
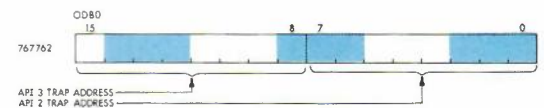
¹ IOT mnemonics do not appear in the assembler symbol table.

² All IOT'S require only one memory cycle. Execute times for IOT'S vary between minimum and maximum limits.

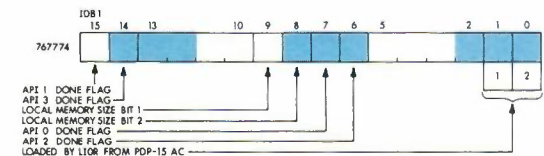
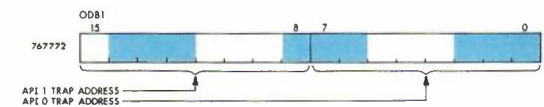
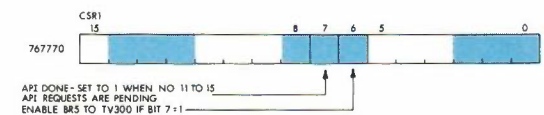
INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

Mnemonic	Code	Operation	Execute Time (Microseconds)
SIOA	706001	Skip if I/O Accepted (done) tests if PDP11 has done DAT1 to 767764 since last LIOR	2.21-3.27
SAPI0	706101	Skip if API 0 flag	2.21-3.27
SAPI1	706121	Skip if API 1 flag	2.21-3.27
SAPI2	706141	Skip if API 2 flag	2.21-3.27
SAPI3	706161	Skip if API 3 flag	2.21-3.27
CIOD	706002	Clear I/O Done (Accepted)	3.21-4.27
CAPI0	706104	Clear API 1 flag	3.96-5.02
CAPI1	706124	Clear API 0 flag	3.96-5.02
CAPI2	706144	Clear API 2 flag	3.96-5.02
CAPI3	706164	Clear API 3 flag	3.96-5.02
—	706004	Load I/O Register PDP11 locations 767764 and bits 1+0 of 767774 Clear I/O Done (Accepted) and Load I/O Register Load Status (AC17→Enable Interrupt Bit) OR Enable Interrupt bit to AC 17	3.96-5.02
LIOR	706006	Read Status (AC17→Enable Interrupt Bit)	3.96-5.02
LDRS	706122	Load Status (AC17→Enable Interrupt Bit)	3.21-4.27
—	706102	OR Enable Interrupt bit to AC 17	3.21-4.27
RDRS	706112	Read Status (enable interrupt bit to AC17)	3.21-4.27

PDP11 Register Definitions



LOADED by LIOR from PDP15 AC DAT1 to this location clears bit 7 of 767760 and sets I/O Done (Accepted) in PDP15



INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

Mnemonic	Code	Operation	Execute Time (Microseconds)
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TYPE KF15 POWER FAILURE DETECTION

PFSF	703201	Skip on power-low flag	2.21-3.27
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TYPE KM15 MEMORY PROTECTION

MPSK	701701	Skip if memory protection violation	2.21-3.27
MPSNE	701741	Skip if violation caused by attempt to address non-existent memory	2.21-3.27
MPCV	701702	Clear memory protection flag	3.21-4.27
MPCNE	701744	Clear non-existent memory flag	3.96-5.02
MPLD	701704	Load boundary register	3.96-5.02
MPEU	701742	Enter user mode	3.21-4.27

TYPE KT15 MEMORY RELOCATION

MPLR	701724	Load relocation register	3.96-5.02
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CONSOLE TELETYPE KEYBOARD

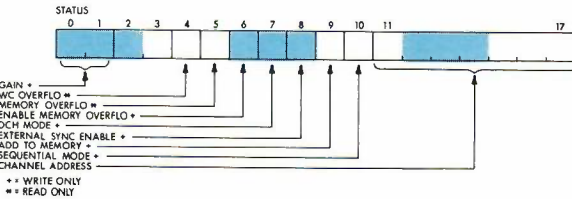
KSF	700301	Skip on keyboard flag	2.21-3.27
—	700302	OR keyboard to AC 10-17	3.21-4.27
KRB	700312	Read keyboard to AC10-17	3.21-4.27
—	700322	OR keyboard to AC10-17 and suppress echo	3.21-4.27
KRS	700332	Read keyboard to AC10-17 and suppress ECHO (Full Duplex made of operation)	3.21-4.27

CONSOLE TELETYPE TELEPRINTER

TSF	700401	Skip on teleprinter flag	2.21-3.27
TCF	700402	Clear teleprinter flag	3.21-4.27
—	700404	Load printer buffer and print	3.96-5.02
TLS	700406	Clear teleprinter flag, load teleprinter buffer and print	3.96-5.02

AD15 ANALOG SUBSYSTEM

ADSF	701301	Skip on AD Done	2.21-3.27
MSSF	701321	Skip on Memory overflow	2.21-3.27
WCSP	701341	Skip on WC overflow	2.21-4.27
ADCF	701362	Clear AD15	3.21-4.27
ADCV	701304	Lead Status and Convert	3.96-5.02



ADRS	701342	Read Status	3.21-4.27
ADRB	701302	Read Data and clear Done	3.96-4.27

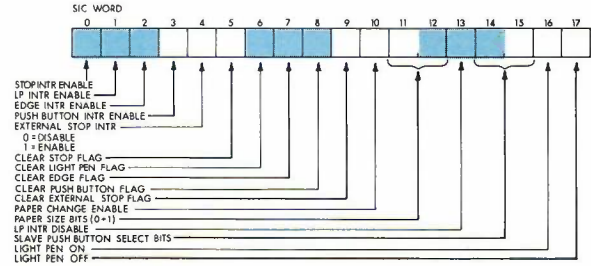
INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

Mnemonic	Code	Operation	Execute Time (Microseconds)
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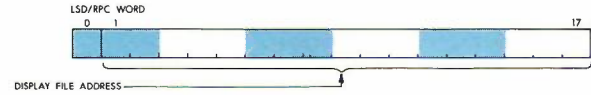
TYPE VT15 DISPLAY PROCESSOR

IOT Central Instruction

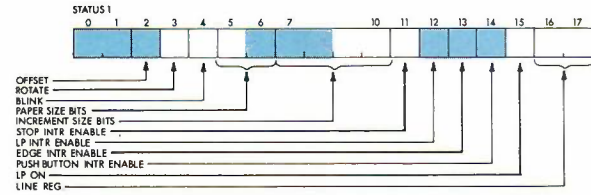
SPSF	703001	Skip on Stop Flag	2.21-3.27
SPLP	703021	Skip on Light Pen flag	2.21-3.27
SPPB	703041	Skip on Push Button flag	2.21-3.27
SPFE	703061	Skip on Edge Flag	2.21-3.27
SPDF	703101	Skip on (any) Display Flag	2.21-3.27
SPDI	703121	Skip on (any) Display Interrupting flag	2.21-3.27
SPES	703161	Skip on External Stop flag	2.21-3.27
SIC	703024	Set Initial Conditions	3.95-5.02



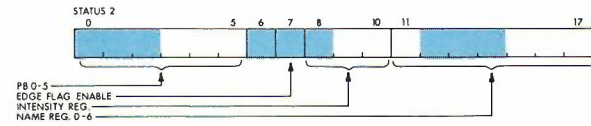
LSD	703004	Load Display Address and Start Display	3.95-5.02
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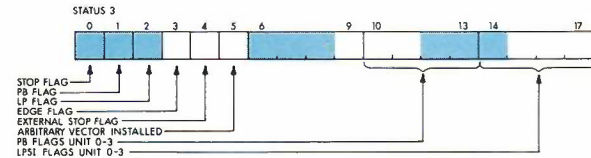
STPD	703044	External Stop Display	3.95-5.02
RESD	703064	Resume Display (from flag)	3.21-3.27
RS1	703002	Read Status 1	3.21-3.27



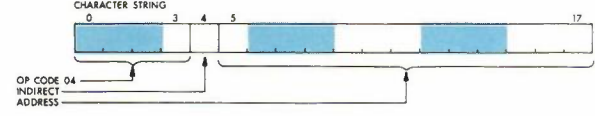
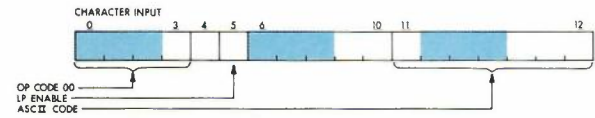
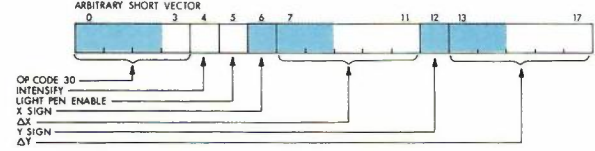
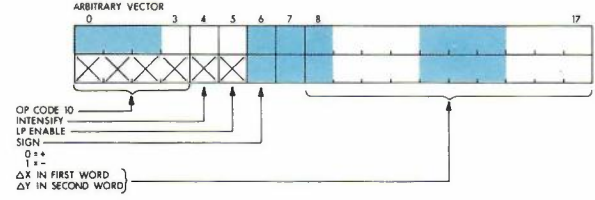
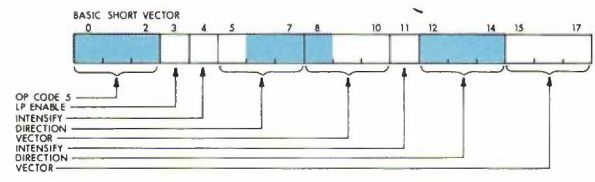
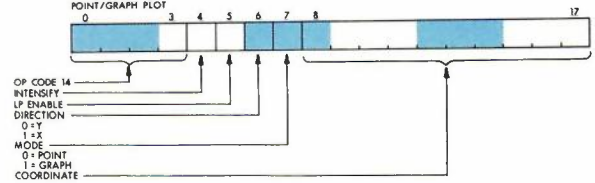
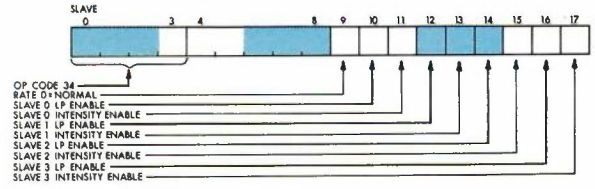
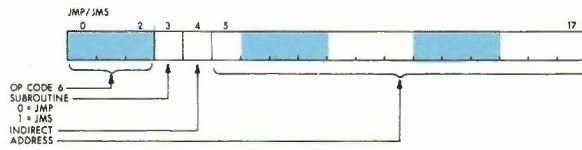
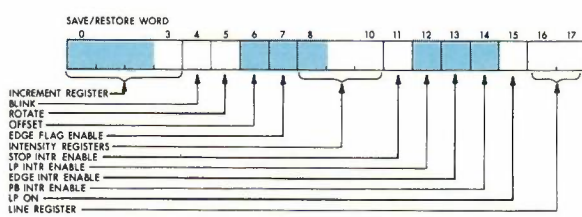
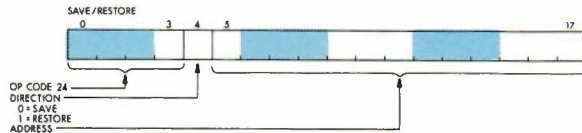
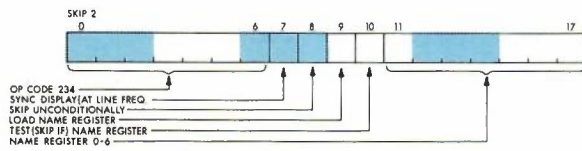
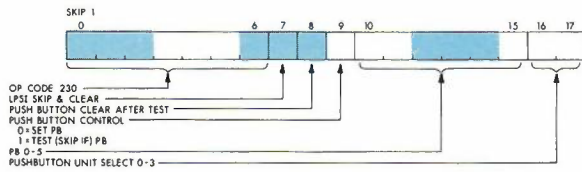
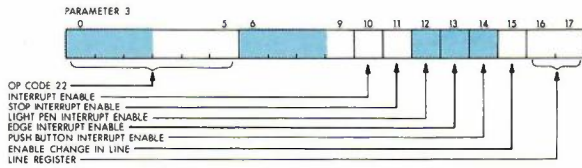
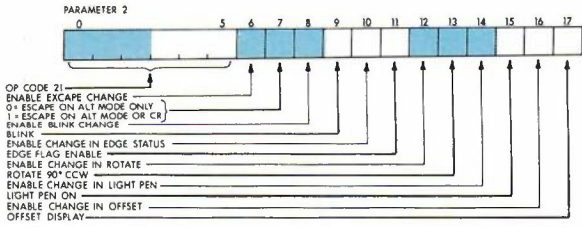
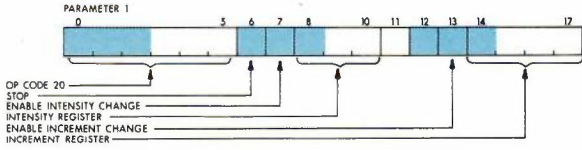
RS2	703022	Read Status 2	3.21-3.27
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RS3	703142	Read Status 3	3.21-3.27
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VT15 INSTRUCTIONS



INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

Mnemonic	Code	Operation	Execute Time (Microseconds)
TYPE VP15A STORAGE TUBE DISPLAY			
SDDF	700521	Skip on display done flag	2.21-3.27
CDDF	700722	Clear display done flag	3.21-4.27
CXB	700502	Clear x-coordinate buffer	3.21-4.27
CYB	700602	Clear y-coordinate buffer	3.21-4.27
EST	700724	Erase storage tube	3.96-5.02
LXB	700504	Load x-coordinate buffer from AC8-17	3.96-5.02
LYB	700604	Load y-coordinate buffer from AC8-17	3.96-5.02
LXBD	700564	Load x-coordinate buffer and display the point specified by XB and YB (store mode)	3.96-5.02
LYBD	700664	Load the y-coordinate buffer and display the point specified by XB and YB (store mode)	3.96-5.02
LXDNS	700544	Load the x-coordinate buffer and display the point specified by XB and YB (non-store mode)	3.96-5.02
LYDNS	700644	Load the y-coordinate buffer and display the point specified by XB and YB (non-store mode)	3.96-5.02

TYPE VP15B, VP15BL, VP15C, VP15CL OSCILLOSCOPE DISPLAYS

DSF	700501	Skip if display (light pen) flag is a 1	2.21-3.27
DCF	700702	Clear display (light pen) flag	3.21-4.27
DLB	700704	Load the brightness register from bits 16-17 of the AC. Note: This instruction clears the display flag associated with the light pen	3.96-5.02
DXC	700502	Clear the x-coordinate buffer	3.21-4.27
DYC	700602	Clear the y-coordinate buffer	3.21-4.27
DXL	700504	Load the x-coordinate buffer from AC8-17	3.96-5.02
DYL	700604	Load the y-coordinate buffer from AC8-17	3.96-5.02
DXS	700544	Load the x-coordinate buffer and display the point specified by the XB and YB	3.96-5.02
DYS	700644	Load the y-coordinate buffer and display the point specified by the XB and YB	3.96-5.02

TYPE XY15 INCREMENTAL PLOTTER CONTROL

PLSF	702401	Skip if plotter flag is a 1	2.21-3.27
PLCF	702402	Clear plotter flag	3.21-4.27
PLPU	702404	Plotter pen up. Raise pen off paper	3.96-5.02
PLPD	702444	Plotter pen down. Lower pen onto paper	3.96-5.02
PLPR	702421	Plotter pen right	2.21-3.27
PLPL	702441	Plotter pen left	2.21-3.27
PLDU	702422	Plotter drum (paper) upward	3.21-4.27
PLDD	702424	Plotter drum (paper) downward	3.96-5.02
PLUD	702442	Plotter drum (paper) upward (same as 702422)	3.21-4.27

INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

Mnemonic	Code	Operation	Execute Time (Microseconds)
RF15/RS09 DECdisk			
DSSF	707001	Skip on disk flag	2.21-3.27
DSCC	707021	Clear the disk control and disable the "freeze" status. A "freeze" is caused either by a timing or data track hardware error or an address parity error. It forces the control to abort the operation in progress.	2.21-3.27
DSCD	707242	Clear the Status Register and Disk Flag	2.21-3.27
DSCF*	707041	Clear the function register and the interrupt mode	3.21-4.27
DSFX*	707042	XOR the contents of AC15, 16, 17 into the function register	3.21-4.27

Function Register	15	16	17	
	FO	F1	INT	
	0	0	X	no effect
	0	1	X	read
	1	0	X	write
	1	1	X	write check

DSCN*	707044	Execute the condition held in the function register	3.96-5.02
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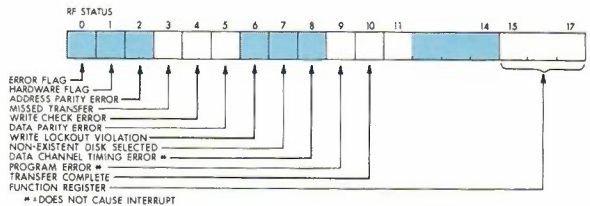
*These instructions may be micro-coded in any combination.



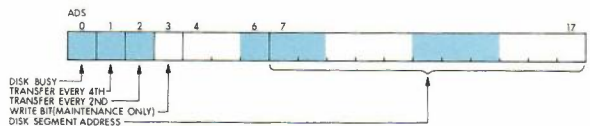
DLAL	707024	Load the contents of the AC into APO	3.96-5.02
DRAL	707022	OR the contents of Address Pointer 0 (APO) into the AC	3.21-4.27



DLAH	707064	Load the contents of the AC into AP1	3.96-5.02
DRAH	707062	OR the contents of Address Pointer 1 (AP1) into the AC	3.96-5.02



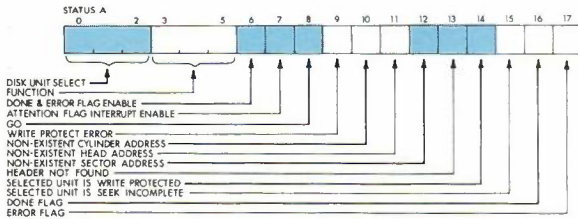
DSRS	707262	OR the Status Register with the AC	3.21-4.27
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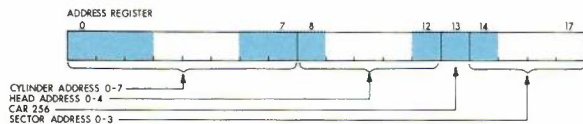
DLOK	707202	OR the disk segment address (ADS) register into the AC	3.21-4.27
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INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

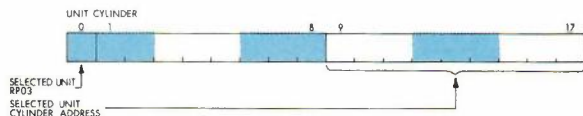
Mnemonic	Code	Operation	Execute Time (Microseconds)
TYPE RP15 DISK PACK CONTROL			
DPSF	706301	Skip on disk flag	2.21-3.27
DPSJ	706341	Skip on job done flag	2.21-3.27
DPSE	706361	Skip on error flag	2.21-3.27
DPSA	706321	Skip on attention flag	2.21-3.27
DPCS	706324	Clear status	3.96-5.02
DPCF	706404	Clear function	3.96-5.02



Function:	0 NOP	4 Seek	
	1 Read	5 Read All	
	2 Write	6 Write All	
	3 Recal	7 Write Check	
DPLF	706464	Load status register A from AC-8 and execute	3.96-5.02
DPLZ	706424	Load AC0-8 zeros into status register A bits 0-8 and execute	3.96-5.02
DPLO	706444	Load the AC0-8 ones into status register A bits 0-8 and execute	3.96-5.02
DPCN	706454	Execute the function register; clear the accumulator	3.96-5.02
DPOSA	706302	OR status register A into the AC	3.21-4.27
DPRSA	706312	Read status register A into the AC	3.21-4.27
DPCA	706344	Load current address register	3.96-5.02
DPOC	706442	OR the current address register into the AC	3.21-4.27
DPRC	706452	Read the current address register into the AC	3.21-4.27
DPWC	706364	Load word count register	3.96-5.02
DPOW	706462	OR the word count register into the AC	3.21-4.27
DPRW	706472	Read the word count register into the AC	3.21-4.27

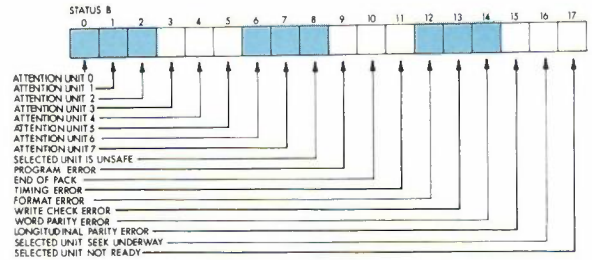


DPLA	706304	Load the cylinder, head, and sector address registers from the AC	3.96-5.02
DPOA	706422	OR the cylinder, head, and sector address register into the AC	3.21-4.27
DPRA	706432	Read the cylinder, head, and sector address into the AC	3.21-4.27



INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

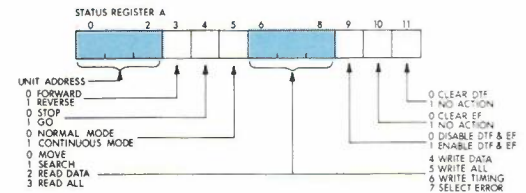
Mnemonic	Code	Operation	Execute Time (Microseconds)
DPOU	706402	OR the unit cylinder address register into the AC	3.21-4.27
DPRU	706412	Read the unit cylinder address register into the AC	3.21-4.27



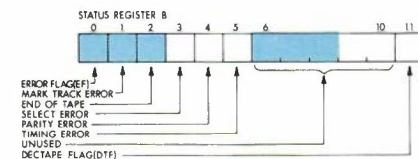
DPOSB	706322	OR status register B into the AC	3.21-4.27
DPRSB	706332	Read status register B into the AC	3.21-4.27

TYPE TC15 DECTAPE CONTROL

DTDF	707601	Skip on DECTape flag	2.21-3.27
DTEF	707561	Skip on error flag	2.21-3.27



DTCA	707541	Clear status register A	2.21-3.27
DTXA	707544	XOR AC into status register A	3.96-5.02
DTLA	707545	Load status register A	3.96-5.02
—	707542	OR status register A → AC00-11	3.21-4.27
DTRA	707552	Read status register A → AC (0-11)	3.21-4.27



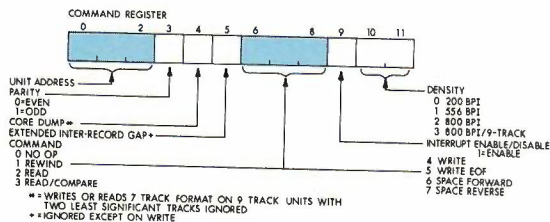
—	707562	OR status register B → AC00-11	3.21-4.27
DTRB	707572	Read status register B	3.21-4.27

INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

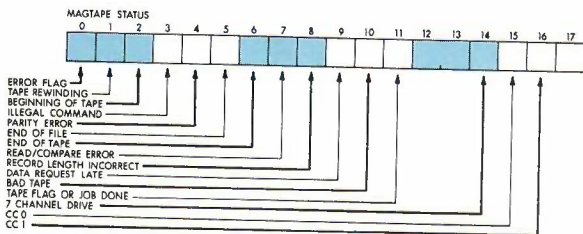
Mnemonic	Code	Operation	Execute Time (Microseconds)
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TYPE TC59D MAGNETIC TAPE CONTROL

MTSF	707341	Skip on error flag (EF) or magnetic tape flag (MTF)	2.21-3.27
MTCR	707321	Skip on tape control ready (TRC)	2.21-3.27
MTTR	707401	Skip on tape transport ready (TUR)	2.21-3.27
MTAF	707322	Clear status and command registers and EF and MTF if TRC. If not, TCR only clears EF and MTF.	3.21-4.27



MTCM	707324	OR ACO-5 and 9-11 into command register. Jam AC6-8	3.96-5.02
MTLC	707326	Load ACO-11 into command register. MTCL is the summation of MTAF and MTCM	3.96-5.02
MTGO	707304	Execute command in command register	3.96-5.02
—	707302	OR command register into ACO-11	3.21-4.27
MTRC	707312	Read command register into ACO-11	3.21-4.27



—	707342	OR status register into ACO-11	3.21-4.27
MTRS	707352	Read status register into ACO-11	3.21-4.27

INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

Mnemonic	Code	Operation	Execute Time (Microseconds)
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TYPE LT15 AND LT19D TELETYPE CONTROL

Teletypewriter

704XX1*	Skip on transmit flag	2.21-3.27
704XX2*	Clear transmit flag	3.21-4.27
704XX4*	Load transmit buffer and send character	3.96-5.02

Keyboard

704XX1*	Skip on receiver flag	2.21-3.27
704XX2*	Read receiver buffer and clear receiver flag	3.21-4.27

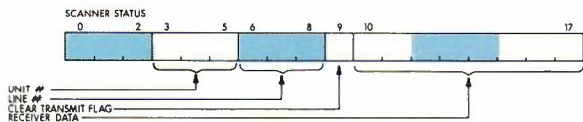
UNIT #	XX (Keyboard)	XX (Teletypewriter)
1	10 (or LT15)	00 (or LT15)
2	12	02
3	14	04
4	16	06
5	30	20

(see PDP-15 User Handbook Vol. II for additional units)

*Where XX is code for Teletype unit

TYPE DC01-ED TERMINAL SCANNER

SSF	704001	Skip on Scanner flag	2.21-3.27
DIS	704004	Disable Scanner (stop Scanner and clear flag)	3.96-5.02



RSD	704002	Read line and data, clear receiver flag and scanner flag	3.21-4.27
LSA	704021	Stop scanner and lead line	2.21-3.27
LSD	704022	Lead transmitter buffer and initiate printing	3.21-4.27
STS	704024	Clear scanner flag and restart at current line	3.96-5.02
—	704027	Stop print and restart	3.96-5.02

For Unit #	Add to basic IOT
0	400
1	440
2	500
3	540

TYPE PC15 PAPER TAPE READER

SPCO	703341	Skip if PC15 installed	3.21-4.27
RSF	700101	Skip on reader flag	2.21-3.27
RCF	700102	OR reader buffer to AC	3.21-4.27
RSA	700104	Select alphanumeric mode	3.96-5.02
RSB	700144	Select binary mode	3.96-5.02
RRB	700112	Read reader buffer	3.21-4.27

TYPE PC15 PAPER TAPE PUNCH

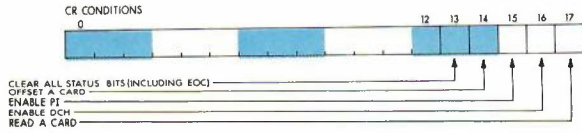
PSF	700201	Skip on punch flag	2.21-3.27
PCF	700202	Clear punch flag	3.21-4.27
PSA	700204	Punch, alphanumeric	3.96-5.02
PSB	700244	Punch, binary	3.96-5.02

INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

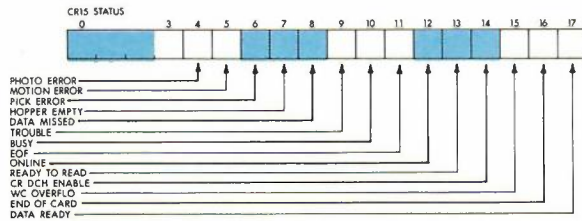
Mnemonic	Code	Operation	Execute Time (Microseconds)
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TYPE CR15 CARD READER CONTROL

CRSKP	706701	Skip on CR15 flag	2.21-3.27
CRPC	706724	Clear CR15 status (except End of Card)	3.96-5.02



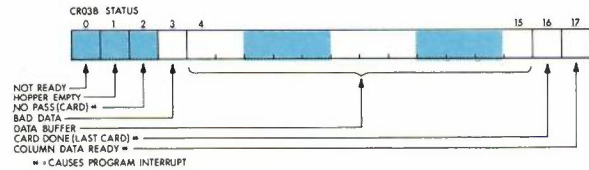
CRLD	706702	OR CR15 Data to AC 06-17	3.21-4.27
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CRLS	706722	OR CR15 Status to AC 04-17	3.21-4.27
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TYPE CR03B CARD READER

CRSI	706721	Skip if card reader interrupt is set	2.21-3.27
CRCS	706704	Clear status register and data buffer	3.96-5.02
CRSC	706722	Clear status register and data buffer; select a card	3.21-4.27



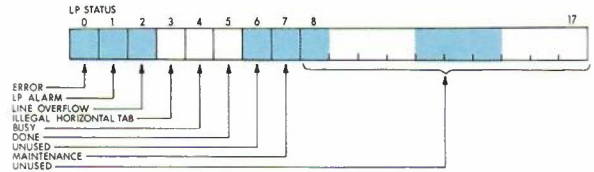
—	706702	OR Data and Status into AC	3.21-4.27
CROR	706712	Load data and status into AC	3.21-4.27

INPUT/OUTPUT TRANSFER INSTRUCTIONS (CONT'D)

Mnemonic	Code	Operation	Execute Time (Microseconds)
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LP15F LINE PRINTER CONTROL

PLSF	706501	Skip on done and error	2.21-3.27
LPCD	706621	Clear done flag	2.21-3.27
LPCS	706641	Clear status and error flags	2.21-3.27
LPEI	706544	Enable interrupt	3.95-5.02
LPDI	706561	Disable interrupt	2.21-3.27
LPP1	706541	Print one Line	2.21-3.27
LPPM	706521	Print Multiple Lines	2.21-3.27



—	706542	OR status 0-7 into AC	3.21-4.27
LPRS	706552	Read status	3.21-4.27

UNICHANNEL DEVICE INFORMATION

Device	Control & Status	Data Buffer	Vec-tor	Prior-ity Level
CR11	Card Reader data buffer 1 data buffer 2	777 160 777 162 777 164	230	BR6
KW11-L	Line Clock	777 546	100	BR6
LA30 (console)	DECwriter keyboard printer	777 560 777 564 777 566	60 64	BR4 BR4
LP11 (LS11)	Line Printer	777 514 777 516	200	BR4
LV11	Printer/Plotter	764 000 764 002	170	BR4
RK11/RK05	Disk Cartridge drive status error control status word count current address disk address maintenance	777 400 777 402 777 404 777 406 777 410 777 412 777 414	220	BR5
XY11 (311)	Plotter	777 254 777 256	120	BR4

PDP-15 IOPS ASCII CHARACTER SET

Listed below is the ASCII character set. Those not interpreted by the ADVANCED Monitor and system programs as meaningful data input or as control characters are marked with an *.

ASCII 7-Bit Octal Code	Char.	ASCII 7-Bit Octal Code	Char.	ASCII 7-Bit Octal Code	Char.	ASCII 7-Bit Octal Code	Char.
000	NUL	040	SP	100	@	140	*'
001	SOH	041	!	101	A	141	*a
002	*STX	042	"	102	B	142	*b
003	ETX	043	#	103	C	143	*c
004	EOT	044	\$	104	D	144	*d
005	*ENQ	045	%	105	E	145	*e
006	*ACK	046	&	106	F	146	*f
007	BEL	047	'	107	G	147	*g
010	*BS	050	(110	H	150	*h
011	HT	051)	111	I	151	*i
012	LF	052	*	112	J	152	*j
013	VT	053	+	113	K	153	*k
014	FF	054	,	114	L	154	*l
015	CR	055	-	115	M	155	*m
016	*SO	056	.	116	N	156	*n
017	*SI	057	/	117	O	157	*o
020	DLE	060	0	120	P	160	*p
021	DC1	061	1	121	Q	161	*q
022	DC2	062	2	122	R	162	*r
023	DC3	063	3	123	S	163	*s
024	DC4	064	4	124	T	164	*t
025	NAK	065	5	125	U	165	*u
026	*SYN	066	6	126	V	166	*v
027	*ETB	067	7	127	W	167	*w
030	CAN	070	8	130	X	170	*x
031	*EM	071	9	131	Y	171	*y
032	SUB	072	:	132	Z	172	*z
033	ESC	073	;	133	[173	*{
034	*FS	074	<	134	\	174	*
035	*GS	075	=	135]	175	ESC
036	*RS	076	>	136	↑ or A	176	ESC
037	*US	077	?	137	← or _	177	DEL

Codes 33, 176, 175 are interpreted as ESC (ALT Mode) and are converted on input to code 175 by IOPS handlers.

Characters in the left hand column are input by pressing the Control (CTRL) key and the corresponding key in column 3.

API Addresses

Break Address	Standard Device	Suggested Priority Level
40	Software channel 0	4
41	Software channel 1	5
42	Software channel 2	6
43	Software channel 3	7
44	DEctape (TC15)	1
45	MagTape (TC59)	1
46		
47		
50	Paper Tape Reader (PC15)	2
51	Clock Overflow (KW15)	3
52	Power Fail (KF15)	0
53		
54	Graphics (VT15/VP15)	2
55	Card Readers (CR15/CR03B)	2
56	Line Printer (LP15)	3
57	A/D (AD15/AF01)	0
60	DB99A/DB98A	3
61		
62	Data Phone (DP09A)	2
63	DECdisk (RF15)	1
64	Diskpack (RP15)	1
65	Plotter (XY15)	1
66		
67		
70	Scanners (DC01-ED) as needed use 70-77	3
71	UDC15	
72	ADC15	
74	LT19 & LT15 Teleprinter	3
75	LT19 & LT15 Keyboard	3
76		
77		

Multi-Cycle Data Channel Addresses

Device	Word Count	Current Address
DEctape TC15	30	31
MagTape TC59	32	33
CR15	22	23
AD15	24	25
AD15	26	27
RF15	36	37
LP15	34	35

CONSOLE REGISTER SELECT

NORMAL

Switch in position:	Register Contents:
AC	Accumulator register
PC	Program Counter register
OA	Operand Address register
MQ	Multiplier Quotient register (EAE Option)
PL/SC	Priority Level/Step Counter
XR	Index Register
LR	Limit Register
EAE	Extended Arithmetic status
DSR	Data Storage Register
I/OB	Input/Output Bus
STA	Input/Output Status (Indicates only when the processor is stopped)
MO	Memory Output register

MAINTENANCE

ABU	A bus
BBU	B bus
CBU	C bus
SFT	Shift bus
I/OA	Input/Output address
SUM	Sum bus (output of adders)
M1	Maintenance word one
M2	Maintenance word two
MDL	Memory data lines
MMa	Memory address
MMB	Memory Buffer
MST	Memory Status